REMARKS

Claims 1 and 11 are amended. Claims 56-62 are added. Claims 1, 4-16 and 56-62 are pending in the application for consideration.

Claims 11-14 stand rejected under 35 USC §112, second paragraph as being indefinite. Claims 1, 4-11 and 13-15 stand rejected under 35 USC §102(b) as being anticipated by Ramakrishnan (U.S. Patent No. 5,192,871). Claims 12 and 16 stand rejected under 35 USC §103 as being unpatentable over Ramakrishnan in view of Graettinger (U.S. Patent No. 5,844,771).

Regarding the §112 rejection, second paragraph, claim 11 is amended to overcome the rejection, and therefore, the rejection should be withdrawn.

Regarding the §102(b) rejection, claim 1 recites a high K substantially crystalline material layer is at least 70% crystalline. Ramakrishnan teaches crystalline films for dielectric materials have higher dielectric constants than amorphous or partially crystalline films of the same material (col.2, lns. 35-39). However, the reference is completely devoid of any teaching to a crystalline percentage for the crystalline films, and therefore, in no reasonable interpretation does Ramakrishnan teach or suggest a high K substantially crystalline material layer is at least 70% crystalline as recited in claim 1. Accordingly, Ramakrishnan fails to

teach a positively recited limitation of claim 1, and therefore, the rejection is overcome. Applicant respectfully requests allowance of claim 1 in the next Office Action.

Claims 4-16 and 56-59 depend from independent claim 1, and therefore, are allowable for the reasons discussed above with respect to the independent claim, as well as for their own recited features which are neither shown or taught by the art of record.

For example, claim 10 recites a high K substantially crystalline material is at least 98% crystalline. Ramakrishnan is completely devoid of any teaching to a crystalline percentage for the crystalline films, and therefore, in no reasonable interpretation does Ramakrishnan teach or suggest that a high K substantially crystalline material layer is at least 98% crystalline as recited in claim 10. Accordingly, Ramakrishnan fails to teach a positively recited limitation of claim 10, and therefore, for at least this additional reason, the rejection is improper and should be withdrawn.

Claim 10 further recites a high K substantially amorphous material layer is at least 98% amorphous. Ramakrishnan is completely devoid of any teaching to an amorphous percentage for the amorphous material, and therefore, in no reasonable interpretation does Ramakrishnan teach or suggest that a high K substantially amorphous material layer is at least 98% amorphous as recited in claim 10. Accordingly, Ramakrishnan fails to teach another positively recited limitation of claim 10, and therefore, for this additional reason, the rejection is

improper and should be withdrawn. Applicant respectfully requests allowance of claim 10 in the next Office Action.

Regarding claim 10, the Examiner states the amorphous material of Ramakrishnan is 100% amorphous without pointing to any teaching in any reference (pg. 4 of paper no. 17). Applicant disagrees with the statement that Ramakrishnan teaches or suggests 100% amorphous material. The asserted referenced, Ramakrishnan, is devoid of any amorphous percentage teachings. The Examiner is reminded that 37 CFR §1.104(d)(2) states when a rejection in an application is based on facts within the personal knowledge of an employee of the Office, the rejection must be supported by an affidavit when called for by the Applicant. No specific reference teachings are cited as allegedly disclosing the amorphous material is 100% in support of the Examiner's rejection. Accordingly, the rejection can only be based upon the personal knowledge of the Examiner. Consequently, Applicants request an affidavit or additional cited art that particularly teaches the limitations of claim 10 if claim 10 is not found to be allowable in the next Action. Without such affidavit or additional art, Applicants are denied an opportunity to properly respond to the rejection due to the lack of prior art or submission of an affidavit. According to 37 CFR §1.104(d)(2), Applicants should be afforded the opportunity to contradict or explain such prior art or affidavit.

This application is now believed to be in immediate condition for allowance, and action to that end is respectfully requested. If the Examiner's next anticipated action is to be anything other than a Notice of Allowance, the undersigned

respectfully requests a telephone interview prior to issuance of any such subsequent action.

Respectfully submitted,

Dated: 4-4-02

By: _____
D. Brent Kenady
Reg. No. 40,045

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 09/512,149
Filing Date ..... February 23, 2000
Inventor ..... Vishnu K. Agarwal
Assignee ..... Micron Technology, Inc.
Group Art Unit 2814
Examiner ..... M. Crespo
Attorney's Docket No. MI22-1322
Title: Integrated Circuitry Including a Capacitor With an Amorphous and a Crystalline High K Capacitor Dielectric Region

VERSION WITH MARKINGS TO SHOW CHANGES MADE ACCOMPANYING RESPONSE TO DECEMBER 5, 2001 OFFICE ACTION

In the Claims

The claims have been amended as follows. Underlines indicate insertions and ~~strikeouts~~ indicate deletions.

1. (Amended) Integrated circuitry comprising a capacitor comprising a first capacitor electrode, a second capacitor electrode and a high K capacitor dielectric region received therebetween; the high K capacitor dielectric region comprising a high K substantially amorphous material layer and a high K substantially crystalline material layer, the high K substantially amorphous material and the high K substantially crystalline material constituting different chemical compositions, the high K substantially crystalline material being received over the high K substantially amorphous material; and

wherein the high K substantially crystalline material layer is at least 70% crystalline.

11. (Amended) The integrated circuitry of claim 1 comprising a semiconductor substrate, the capacitor being received at least partially over the semiconductor substrate, the high K substantially ~~crystalline~~ amorphous material layer being received between the semiconductor substrate and the high K substantially ~~amorphous~~ crystalline material layer.

New Claims:

56. (New) The integrated circuitry of claim 1 wherein the high K substantially amorphous material layer is at least 70% amorphous.

57. (New) The integrated circuitry of claim 1 further comprising a substrate supporting the first and second capacitor electrodes, and an insulative layer intermediate the substrate and the first and second capacitor electrodes.

58. (New) The integrated circuitry of claim 57 wherein the insulative layer comprises an oxide layer.

59. (New) The integrated circuitry of claim 57 wherein the insulative layer comprises silicon dioxide.

60. (New) The integrated circuitry of claim 1 wherein the high K substantially amorphous material layer comprises a thickness in a range of about 20 Ångstroms to about 250 Ångstroms.

61. (New) The integrated circuitry of claim 1 wherein the high K substantially crystalline material layer comprises a thickness in a range of about 20 Ångstroms to about 90 Ångstroms.

62. (New) The integrated circuitry of claim 1 wherein the high K capacitor dielectric region comprises a thickness in a range of about 40 Ångstroms to about 500 Ångstroms.

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